REMARKS

The claims remaining in the present application are Claims 1-13. Claims 1, 2, 4 - 7, 11, and 13 have been amended. The Title of the instant specification has been amended. No new matter has been added as a result of these amendments.

Title of the Specification

The Title of the instant specification has been amended. Applicants respectfully request that the examiner review and approve of the amended Title.

35 U.S.C. §102

Claims 1-13 are rejected under 35 U.S.C. §102(e) as being anticipated by Orton et al., U.S. Patent No. 6,118,306 (hereinafter, Orton). The rejection is respectfully traversed for the following reasons.

Currently Amended Independent Claim 1 recites, in part:

> reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled, wherein said value of the core voltage is not sufficient to maintain processing activity in said processor.

Amended Independent Claim 1 recites that the core voltage is reduced to a value that is sufficient to maintain state of the processor, but is not sufficient to maintain processing activity in the processor. Applicants assert that reducing a voltage to a processor to a level that is sufficient to maintain state of the processor, but is not sufficient to maintain processing activity in the processor, would not have been obvious to one of ordinary skill in the art at the time of Applicants' invention based on the cited art of record. Applicants do not believe that Orton teaches or suggests reducing the voltage of the processor core to a value that is sufficient to maintain state of the processor, but is not sufficient to maintain processing activity in the processor.

Orton may purport to disclose a system that places a processor into a low activity state. During this state, the frequency of operation may be reduced. Orton may also disclose that a high and a low voltage may be applied to the processor. However, Applicants have found nothing in Orton that expressly teaches or suggests that one of the two voltages is sufficient to maintain state of the processor, but is not sufficient to maintain processing activity in the processor, as Applicants have claimed. Orton does provide exemplary high and low voltage values at col. 7, lines 63-65. Specifically, these values are 1.3V and 1.8V. It is Applicants' understanding that both of these values were typical values that would have been sufficient to maintain processor activity given Orton.

Thus, Orton is silent as to teaching reducing voltage to a value that is sufficient to maintain state of the processor, but is not sufficient to maintain processing activity in the processor. Moreover, Orton's only exemplary voltages would have been sufficient to maintain processor activity, according to Applicants' understanding. Therefore, Applicants respectfully assert that Orton fails to teach or suggest reducing voltage to a value that is sufficient to maintain state of the processor, but is not sufficient to maintain processing activity in the processor, as the Applicants have claimed.

For the foregoing reason, Claim 1 is neither taught nor suggested by Orton. Therefore, Applicants respectfully request allowance of Claim 1.

Currently Amended Independent Claim 7 recites, in part:

> means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in a computing mode, wherein the level less than that for operating the processor in a computing mode is sufficient to maintain state of the processor (emphasis added).

For at least the reasons discussed in the response to Claim 1, Claim 7 also overcomes Orton. As such, Applicants earnestly request allowance of Claim 7.

Claims 2-3, 8-9, and 10 depend from Claims 1 and 7, which are believed to be allowable for the foregoing reasons. As a result of their dependency on claims believed to be allowable, Claims 2-3, 8-9, and 10 are believed to be allowable. Applicants earnestly request their allowance.

CLAIM 4

Currently Amended Claim 4 recites, in part:

> reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled by
>
> furnishing an input to reduce an output voltage provided by a voltage regulator furnishing core voltage to the processor, and
>
> providing a feedback signal to the voltage regulator to reduce its output voltage below a specified output voltage (emphasis added).

Claim 4 has been rewritten in independent form including all limitations from its base claim and intervening claim. Applicants do not intend that the scope of Claim 4 is narrowed by this amendment. Independent Claim 4 recites that a feedback signal is provided to the voltage regulator to reduce its output voltage below a specified output voltage. Applicants respectfully assert that Orton fails to teach or suggest this claimed limitation.

The passages in Orton to which the rejection refers may teach that a signal is applied to a voltage regulator to alter its output voltage. However, Applicants have claimed that a feedback signal is applied to the voltage regulator. In Figure 1 of Orton,

the voltage regulator (52) is depicted with an input signal from the host bridge (18). However, Applicants do not understand the voltage regulator to receive a feedback signal, as Applicants have claimed.

In Figure 5 of Orton, the voltage regulator (52) has its output voltage controlled by the VR_LO/HI# signal from the NB control logic (400). The voltage regulator also receives a signal from the system electronics (VR_ON), which directs the voltage regulator to settle to the voltage level selected by the VR_LO/HI# signal (col. 7, lines 59-63). Applicants do not understand either of these inputs to the voltage regulator to be feedback signals, as claimed. Furthermore, Applicants do not understand either of these signals to reduce its output voltage below a specified output voltage, as claimed.

For the foregoing reasons, Applicants assert that Independent Claim 4 is neither taught nor suggested by Orton. Consequently, Applicants earnestly request that Claim 4 be allowed.

CLAIMS 5 and 6

Independent Claim 5 recites, in part:

> transferring operation of a voltage regulator furnishing core voltage in a mode in which power is dissipated during reductions in core voltage to a mode in which power is saved during a voltage transition when it is determined that a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled.

Claim 5 has been rewritten in independent form including all limitations from its base claim and intervening claim. Applicants do not intend that the scope of Claim 5 is narrowed by this amendment. Independent Claim 5 recites that an operation of a voltage regulator is transferred from a mode in which power is dissipated to a mode in

which power is saved. Claim 5 recites an embodiment that operates a voltage regulator in two modes. A first of those modes is one in which power is dissipated and a second mode is one in which power is saved. Claim 5 recites that the voltage regulator is operated in the power saving mode during a voltage transition.

Applicants respectfully assert that Orton fails to teach or suggest the limitations of Claim 5. Orton may discuss reducing power consumption (see, e.g., col. 2, lines 18-20). Orton may achieve a reduction in power by, for example, reducing the operating frequency of the processor. However, power savings can be achieved in manners other than reducing frequency and/or reducing voltage. Applicants have specifically recited in this embodiment that saving power is performed by a choice of mode of operation of the voltage regulator. Orton is silent as to operating the voltage regulator in two different modes, as claimed. Thus, Orton fails to teach or suggest the claimed transferring the operation of a voltage regulator from a mode in which power is dissipated to a mode in which power is saved, during a voltage transition.

For the foregoing reasons, Orton fails to teach or suggest the limitations of Claim 5. Therefore, Applicants earnestly request allowance of Claim 5.

Claim 6 depends from Claim 5. By virtue of its dependency on a claim that is believed to be allowable, Applicants believe Claim 6 to be allowable. Claim 6 is believed to be allowable for the following additional reason.

Claim 6 recites, in part:

> returning the voltage regulator to its original mode of operation when the value of the core voltage sufficient to maintain state during the mode in which system clock is disabled is reached.

Claim 6 recites the limitation of returning the voltage regulator to its original mode of operation when the value of the core voltage sufficient to maintain state during the mode in which system clock is disabled is reached. As Applicants have previous argued, Orton fails to discuss operating a voltage regulator in two modes of operation, one in which power is dissipated and another mode in which power is saved. Therefore, Orton cannot teach or suggest the claimed limitation of "returning the voltage regulator to its original mode of operation when the value of the core voltage sufficient to maintain state during the mode in which system clock is disabled is reached."

For the foregoing reasons, Orton fails to teach or suggest the limitations of Claim 6. Therefore, Applicants earnestly request allowance of Claim 6.

Claims 11 and 12

Amended Independent Claim 11 recites, in part:

> a voltage regulator having:
>
> an output terminal providing a selectable voltage, and
>
> an input terminal for receiving signals indicating the selectable voltage level;
>
> ...
>
> means for reducing the selectable voltage below a level provided by the voltage regulator (emphasis added).

Claim 11 has been rewritten in independent form including all limitations from its base claim and intervening claim. Applicants do not intend that the scope of Claim 11 is narrowed by this amendment. Claim 11 recites a "means for reducing the selectable voltage below a level provided by the voltage regulator." Thus, the voltage regulator is recited as having an output terminal that provides a selectable voltage. Furthermore, Claim 11 recites that the selectable voltage can be reduced below a level that the

voltage regulator provides. This allows embodiments of the present invention to provide a voltage to a processor that is below that which the voltage regulator provides.

Applicants have reviewed Orton and respectfully assert that Orton fails to teach or suggest, "means for reducing the selectable voltage below a level provided by the voltage regulator." The rejection has rejected Claim 11 for the same reasons as Claim 4, according to Applicants understanding of the rejection. The Applicants respectfully assert that Orton fails to teach or suggest a structure that provides the claimed function of reducing the selectable voltage below a level provided by the voltage regulator.

For example, in Figure 5 of Orton, the voltage regulator (52) has its output voltage controlled by the VR_LO/HI# signal from the NB control logic (400). The voltage regulator also receives a signal from the system electronics (VR_ON), which directs the voltage regulator to settle to the voltage level selected by the VR_LO/HI# signal (col. 7, lines 59-63). Applicants do not understand either of these inputs to the voltage regulator to provide the necessary structure to reduce the output voltage of the voltage regulator below a *specified* output voltage, as claimed.

For the foregoing reasons, Orton fails to teach or suggest the limitations of Claim 11. Therefore, Applicants earnestly request allowance of Claim 11.

Claim 12 depends from Claim 11. By virtue of its dependency on a claim that is believed to be allowable, Applicants believe Claim 12 to be allowable. Claim 12 is believed to be allowable for the following additional reasons.

Claim 12 recites:

> A circuit as claimed in Claim 11 in which the means for reducing the selectable voltage below a level provided by the voltage regulator comprises:
>
> a voltage divider network joined between the output terminal and a voltage source furnishing a value higher than the selectable voltage, and
>
> a voltage regulator feedback circuit receiving a value from the voltage divider network.

Claim 12 recites elements coupled to the output terminal and a voltage source that furnishes a higher voltage than the selectable voltage. Applicants have reviewed Orton and respectfully assert that Orton fails to teach or suggest this limitation. Moreover, the rejection fails to point out where Orton teaches or suggests such a limitation. This is because the rejection references the rejection of Claims 1-6 when discussing the rejection to Claim 12. However, the limitation of a voltage divider network joined between the output terminal and a voltage source furnishing a value higher than the selectable voltage are not recited in any of Claims 1-6.

Claim 12 further recites, "a voltage regulator feedback circuit receiving a value from the voltage divider network." Applicants have reviewed Orton and respectfully assert that Orton fails to teach or suggest this limitation. Moreover, the rejection fails to point out where Orton teaches or suggests such a limitation. This is because the rejection references the rejection of Claims 1-6 when discussing the rejection to Claim 12. However, the limitation of a voltage regulator feedback circuit receiving a value from the voltage divider network." is not recited in any of Claims 1-6.

For the foregoing reasons, Orton fails to teach or suggest the limitations of Claim 12. Therefore, Applicants earnestly request allowance of Claim 12.

CLAIM 13

Claim 13 recites, in part:

> a voltage regulator having:
>
> an output terminal providing a selectable voltage, and
>
> an input terminal for receiving signals indicating the selectable voltage level;
>
> ...
>
> circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases, and
>
> means for enabling the circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases (emphasis added).

Claim 13 has been rewritten in independent form including all limitations from its base claim and intervening claim. Applicants do not intend that the scope of Claim 13 is narrowed by this amendment. Claim 13 recites circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases. Claim 13 further recites means for enabling this circuitry.

Applicants respectfully assert that Orton fails to teach or suggest the limitations of Claim 13. Orton may discuss reducing power consumption (see, e.g., col. 2, lines 18-20). Orton may achieve a reduction in power by, for example, reducing the operating frequency of the processor. However, power savings can be achieved in manners other than reducing frequency and/or reducing voltage. Applicants have specifically recited operating the voltage regulator in two different modes. Orton is silent as to circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases, as claimed.

Applicants further note that the rejection fails to point out where Orton teaches or suggests such a limitation. This is because the rejection references the rejection of

Claims 1-6 when discussing the rejection to Claim 13. However, the limitation of circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases is not recited in any of Claims 1-6. Therefore, the rejection fails to discuss this claimed limitation.

For the foregoing reasons, Orton fails to teach or suggest the limitations of Claim 13. Therefore, Applicants earnestly request allowance of Claim 13.

CONCLUSION

In light of the above listed amendments and remarks, allowance of Claims 1-13 is requested.

Should the Examiner have a question regarding the instant amendment and response, the Applicants invite the Examiner to contact the Applicants' undersigned representative at the below listed telephone number.

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